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(19) United States

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Lindholm et al. (43) Pub. Date: Jan. 30, 2003

(54) METHOD, APPARATUS AND ARTICLE OF MANUFACTURE FOR A SEQUENCER IN A TRANSFORM/LIGHTING MODULE CAPABLE OF PROCESSING MULTIPLE INDEPENDENT EXECUTION THREADS

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(21) Appl. No.: **10/177,051**

(22) Filed: **Jun. 21, 2002**

Related U.S. Application Data

(62) Division of application No. 09/456,104, filed on Dec. 6, 1999.

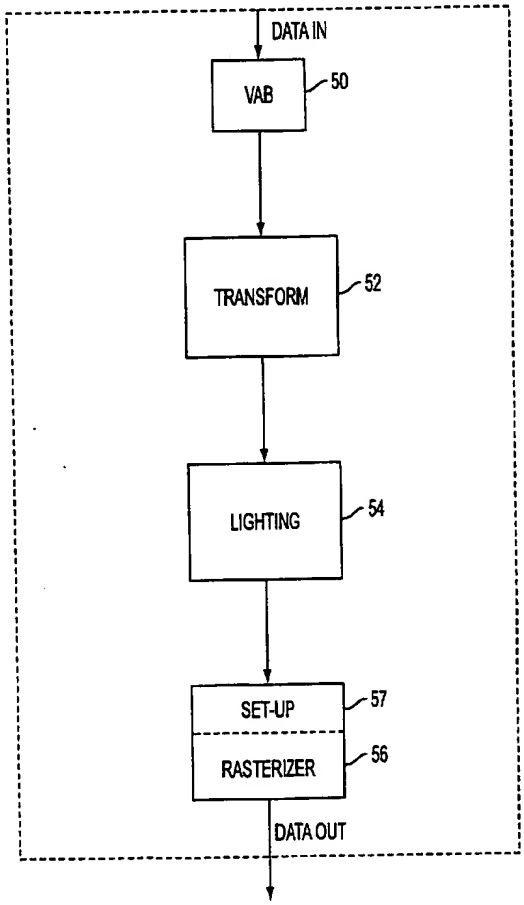
Publication Classification

(51) **Int. Cl.**[7] **G06T 1/20**

(52) **U.S. Cl.** **345/506**

(57) **ABSTRACT**

A method, apparatus and article of manufacture are provided for sequencing graphics processing in a transform or lighting operation. A plurality of mode bits are first received which are indicative of the status of a plurality of modes of process operations. A plurality of addresses are then identified in memory based on the mode bits. Such addresses are then accessed in the memory for retrieving code segments which each are adapted to carry out the process operations in accordance with the status of the modes. The code segments are subsequently executed within a transform or lighting module for processing vertex data.



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(12) Patent Application Publication (10) Pub. No.: US 2002/0196259 A1

Lindholm et al. (43) Pub. Date: Dec. 26, 2002

(54) SINGLE SEMICONDUCTOR GRAPHICS PLATFORM WITH BLENDING AND FOG CAPABILITIES

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(21) Appl. No.: **10/186,557**

(22) Filed: **Jun. 28, 2002**

Related U.S. Application Data

(63) Continuation of application No. 09/960,004, filed on Sep. 20, 2001, which is a continuation of application No. 09/730,652, filed on Dec. 5, 2000, now Pat. No. 6,342,888, which is a continuation of application No. 09/454,516, filed on Dec. 6, 1999, now Pat. No. 6,198,488.

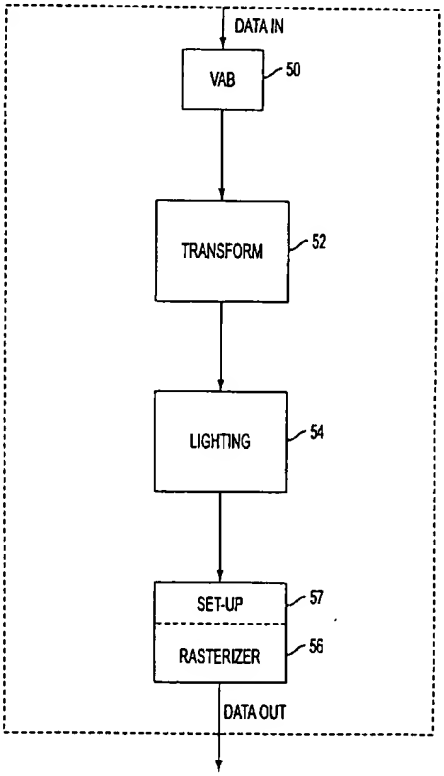
Publication Classification

(51) **Int. Cl.**[7] **G06T 1/20**

(52) **U.S. Cl.** **345/506**

(57) **ABSTRACT**

A graphics pipeline system and associated method are provided for graphics processing. Such system includes a transform module adapted for receiving graphics data. The transform module serves to transform the graphics data from a first space to a second space. Coupled to the transform module is a lighting module which is positioned on the single semiconductor platform for lighting the graphics data. During use, the graphics pipeline system is capable of carrying out a fog and blending operation.



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(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0105519 A1

Lindholm et al. (43) Pub. Date: Aug. 8, 2002

(54) CLIPPING SYSTEM AND METHOD FOR A GRAPHICS PROCESSING FRAMEWORK EMBODIED ON A SINGLE SEMICONDUCTOR PLATFORM

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(21) Appl. No.: **09/957,746**

(22) Filed: **Sep. 20, 2001**

Related U.S. Application Data

(63) Continuation of application No. 09/730,652, filed on Dec. 5, 2000, now patented.

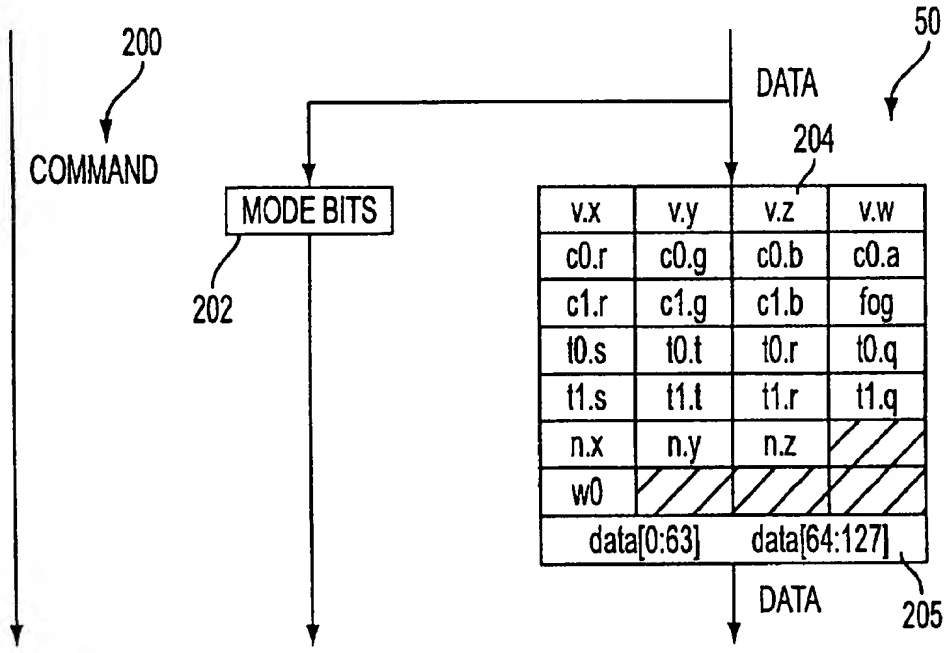
Publication Classification

(51) **Int. Cl.**[7] **G06T 15/50**; G06T 15/60; G06T 1/20; G06F 13/14

(52) **U.S. Cl.** **345/426**; 345/506; 345/519

(57) **ABSTRACT**

A graphics pipeline system is provided for graphics processing. Such system includes a transform module adapted for being coupled to a vertex attribute buffer for receiving vertex data. The transform module serves to transform the vertex data from object space to screen space. Coupled to the transform module is a lighting module which is positioned on the single semiconductor platform for performing lighting operations on the vertex data received from the transform module. Also included is a rasterizer coupled to the lighting module and positioned on the single semiconductor platform for rendering the vertex data received from the lighting module.



US 20020047846A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0047846 A1

Lindholm et al. (43) Pub. Date: Apr. 25, 2002

(54) SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR PERFORMING A SCISSOR OPERATION IN A GRAPHICS PROCESSING FRAMEWORK EMBODIED ON A SINGLE SEMICONDUCTOR PLATFORM

(76) Inventors: **John Erik Lindholm**, Cupertino, CA (US); **Simon Moy**, Mountain View, CA (US); **Kevin Dawallu**, Sunnyvale, CA (US); **Mingjian Yang**, Sunnyvale, CA (US); **John Montrym**, Los Altos, CA (US); **David B. Kirk**, San Francisco, CA (US); **Paolo E. Sabella**, Pleasanton, CA (US); **Matthew N. Papakipos**, Palo Alto, CA (US); **Douglas A. Voorhies**, Menlo Park, CA (US); **Nicholas J. Foskett**, Mountain View, CA (US)

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(21) Appl. No.: **09/961,228**

(22) Filed: **Sep. 20, 2001**

Related U.S. Application Data

(63) Continuation of application No. 09/730,652, filed on Dec. 5, 2000. Continuation of application No. 09/454,516, filed on Dec. 6, 1999, now Pat. No. 6,198,488.

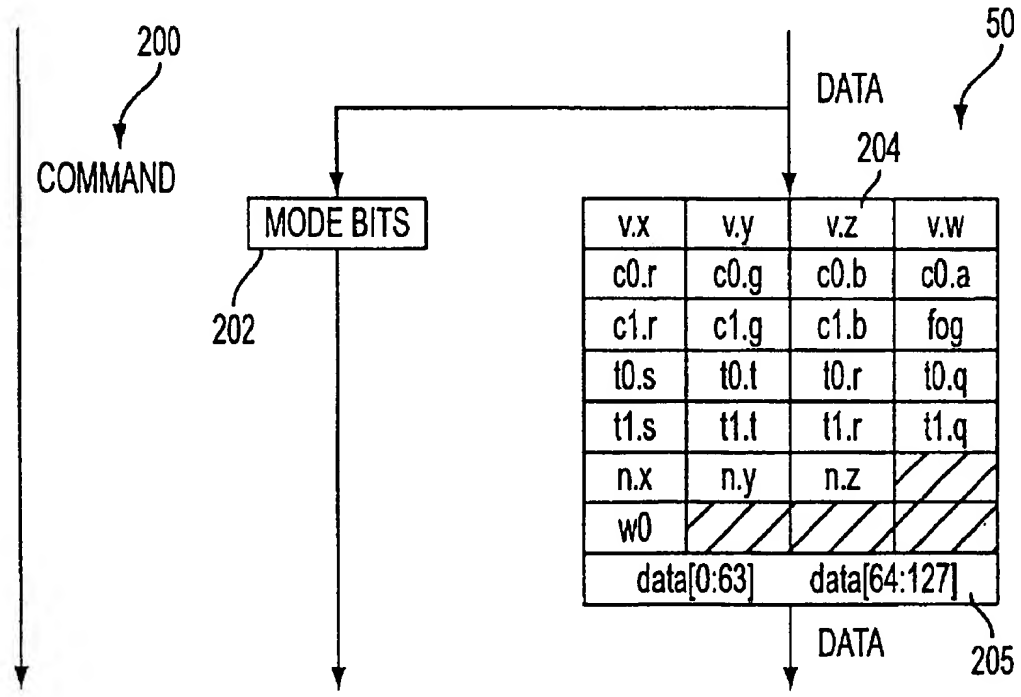
Publication Classification

(51) **Int. Cl.**[7] **G06T 15/50**; G06T 15/60; G06T 1/00; G06T 15/00

(52) **U.S. Cl.** **345/522**; 345/426

(57) **ABSTRACT**

A graphics pipeline system is provided for graphics processing. Such system includes a transform module adapted for being coupled to a vertex attribute buffer for receiving vertex data. The transform module serves to transform the vertex data from object space to screen space. Coupled to the transform module is a lighting module which is positioned on the single semiconductor platform for performing lighting operations on the vertex data received from the transform module. Also included is a rasterizer coupled to the lighting module and positioned on the single semiconductor platform for rendering the vertex data received from the lighting module.



US006515671B1

(12) **United States Patent**
Lindholm et al.

(10) **Patent No.: US 6,515,671 B1**
(45) **Date of Patent: Feb. 4, 2003**

(54) **METHOD, APPARATUS AND ARTICLE OF MANUFACTURE FOR A VERTEX ATTRIBUTE BUFFER IN A GRAPHICS PROCESSOR**

(75) Inventors: **John Erik Lindholm**, Cupertino, CA (US); **Simon Moy**, Mountain View, CA (US)

(73) Assignee: **Nvidia Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/454,525**

(22) Filed: **Dec. 6, 1999**

(51) **Int. Cl.**[7] **G06T 1/20**; G06T 1/00; G06T 15/00

(52) **U.S. Cl.** **345/506**; 345/522

(58) **Field of Search** 345/553, 615, 345/627, 506

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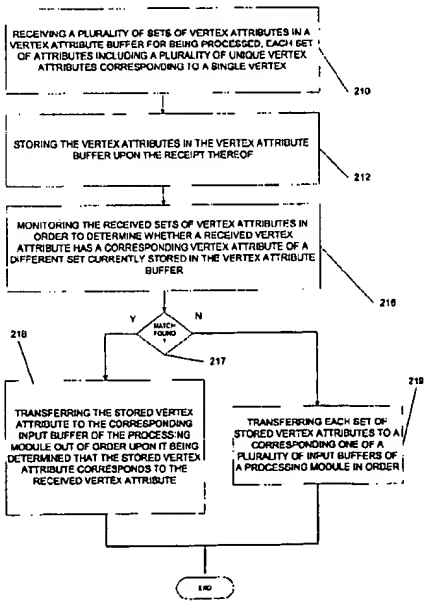
Primary Examiner—Matthew C. Bella
Assistant Examiner—Dalip K. Singh
(74) *Attorney, Agent, or Firm*—Silicon Valley IP Group, LLC.; Kevin J. Zilka

(57) **ABSTRACT**

A method, apparatus and article of manufacture are provided for managing vertex data in a vertex buffer. First, vertex data is received and stored in the vertex buffer. Thereafter, the vertex data is outputted from the vertex buffer to a processing module. During operation, a plurality of command bits is passed from the vertex buffer for determining a manner in which the vertex data is inputted and processed in the input buffer of the processing module. Such command bits are received from a command bit source. Further, a plurality of mode bits indicative of a status of a plurality of modes of process operations is passed. Such mode bits are received from a mode bit source. The mode bits are adapted for determining a manner in which the vertex data is processed in the processing module.

21 Claims, 44 Drawing Sheets



US006492989B1

(12) **United States Patent**
Wilkinson

(10) **Patent No.: US 6,492,989 B1**
(45) **Date of Patent: Dec. 10, 2002**

(54) **COMPUTER METHOD AND APPARATUS FOR CREATING VISIBLE GRAPHICS BY USING A GRAPH ALGEBRA**

(75) Inventor: **Leland Wilkinson**, Chicago, IL (US)

(73) Assignee: **Illumitek Inc.**, Herndon, VA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/553,507**

(22) Filed: **Apr. 20, 2000**

Related U.S. Application Data

(60) Provisional application No. 60/130,234, filed on Apr. 21, 1999.

(51) **Int. Cl.**[7] **G06F 15/00**

(52) **U.S. Cl.** **345/440**; 345/468; 345/586; 345/643

(58) **Field of Search** 345/424, 425, 345/427, 440, 441, 468, 469, 418, 586–587, 606, 610, 616, 643, 644, 673–674, 440.1, 440.2, 467, 475; 704/9; 707/532, 531, 585

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Primary Examiner—Matthew Luu
Assistant Examiner—Wesner Sajous
(74) *Attorney, Agent, or Firm*—Ryndak & Suri

(57) **ABSTRACT**

A computer method, apparatus and storage medium is provided for creating quantitative aesthetic graphics from data. The invention utilizes a graph algebra to construct graphs and visually or otherwise represents the graphs as a quantitative aesthetic graphic representation. To create the quantitative aesthetic graphics from data, the data is indexed to form a data set. Thereafter, the data is converted into a variable data structure composed of an index set, a range and a function. The variable data structure is converted into a variable set by using at least one of a blend step, a cross step and a nest step. The variable set is mapped into a set of points and the set of points is mapped into an aesthetic representation.

63 Claims, 18 Drawing Sheets